



T.J. Krutsick 10

\$2811

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Thomas J. Krutsick
Case: 10
Serial No.: 10/061,475
Filing Date: February 1, 2002
Group: 2811
Examiner: Steven Ho Yin Loke

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: Lisa L. Tulpis Date: July 3, 2003

Title: Method of Fabricating Complementary
Self-Aligned Bipolar Transistors

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AMENDMENT TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is the following document relating to the above-identified patent application:

(1) Amendment and Response to Office Action.

There is an additional claim fee of \$168 due in conjunction with the Amendment. Please charge **Ryan, Mason & Lewis Deposit Account No. 50-0762** the amount of \$168. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter is enclosed.

Respectfully submitted,

Wayne L. Ellenbogen

Date: July 3, 2003

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Signature: *Lisa L. Vulpis* Date: July 3, 2003

#9/A
And
J. Krutsick
7/12/03

Title: Method of Fabricating Complementary Self-Aligned Bipolar Transistors

AMENDMENT AND RESPONSE TO OFFICE ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

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In response to the Office Action dated April 9, 2003, please amend the above-identified application as follows:

IN THE ABSTRACT

Please delete the abstract beginning at page 26, line 2, and replace it with the following rewritten abstract:

--Complementary bipolar transistors are fabricated on a semiconductor wafer by forming, on an upper surface of the semiconductor wafer, a first electrode corresponding to a first transistor, and a second electrode corresponding to a second transistor which is complementary to the first transistor. A first impurity is selectively introduced into⁵⁰ the first and second electrodes. A third electrode corresponding to the first transistor is formed, the third electrode being self-aligned with and electrically isolated from the first electrode, and a fourth electrode is formed corresponding to the second transistor, the fourth electrode being self-aligned with and electrically isolated¹⁰⁰ from the second electrode. A second impurity is selectively introduced into the third and fourth electrodes.

A first active region of the first transistor and a first active region of the second transistor are formed,

A1